globetech SOLUTIONS

Verification Intellectual Property Products

UART *e*VC

e Verification Components

Globetech Solutions' *e*VCs are independent, pre-verified, re-usable, verification environments that can be readily integrated into your design.

Maintaining full compatibility with Cadence's Incisive Specman Simulator™, these components provide a solid basis for forming and realizing a complete, reliable and re-usable verification strategy.

e Reuse Methodology

Globetech Solutions' *e*VCs comply with Cadence's *e* Reuse Methodology (*e*RM™). The *e*RM ensures that *e*VCs seamlessly plug-and-play and operate consistently with all *e*RM compliant verification environments by applying consistent terminology, architecture, coding style and packaging.

Why *e*VCs?

There are many advantages to choosing a Globetech Solutions *e* Verification Component:

- **Time to silicon -** dramatically reduce the verification cycle
- **Flexibility -** quickly create and fine tune a variety of test scenarios
- **Risk Management -** pre-verified components help reduce problem space
- **Re-usability -** spend your time creating new tests, not environments!
- **Full Support -** integration, training and support to ensure your success

The UART *e*VC

The Universal Asynchronous Receiver Transmitter (UART) *e*VC is a powerful verification bundle built around the UART industry standard. Adopted by companies worldwide as a building block for reusable verification platforms, the UART *e*VC can be integrated in a variety of testing scenarios involving a processor and modem/network, making it ideal for embedded processor applications or system-on-chip environments.

Features

- ☑ Compatible with virtually any UART interface
- ☑ Written in *e* and fully compatible with Cadence Incisive Specman Simulator - HDL independent
- ☑ *e*RM compliant - Plug-n-Play
- ☑ Includes executable verification plan for Incisive Verification Manager™
- ☑ Optimized for Incisive Scenario Builder™
- ☑ Interface-level: Can be used to verify the serial interface behavior of any UART device
- ☑ Serial interface agent provides constrained-random UART frame sequence generation with error injection
- ☑ Programmable serial interface characteristics with auto-flow support
- ☑ Independent monitor supports re-usability in different verification environments without loss of coverage
- ☑ Fault start bit and break indication detection
- ☑ Built-in metric analysis for Coverage-Driven Verification (CDV)
- ☑ Complete and configurable error reporting, adjustable levels of tracing and verbosity
- ☑ IrDA® SIR frame encoding/decoding for UART-over-IrDA support [provided as separate module]

UART *e*VC Structure

The UART *e*VC is a universal, highly reusable verification component, providing advanced capabilities for generating UART frames, driving and monitoring a UART interface, detecting errors and estimating functional coverage.

Verification Using the UART *e*VC

In **Figure 1**, the UART *e*VC is used to verify the serial interface of a UART device. The device could be a standalone IP core or part of a larger System on Chip design under test. In this scenario, the *e*VC's *serial agent* initiates constrained-random sequences to the DUT. The *monitor* examines traffic, scoreboards data and utilizes the *checker* to ensure adherence to the UART protocol. The *coverage* module on-the-fly tracks the functional aspects of the protocol that have been exercised. The *e*VC makes no assumptions as to the device's architecture or processor interface, making it applicable to virtually any type of UART.

Benefits of the UART *e*VC

- ☑ **Universal solution:** A powerful verification environment which can be used with any UART device
- ☑ **Solid technology:** Built on best-of-breed technology and methodologies by Cadence Design Systems
- ☑ **Proven quality:** In strict compliance with industry quality standards
- ☑ **High maturity:** Used in many silicon-proven projects and a standard for many technology developers
- ☑ **Maximum reuse:** An *e*RM-compliant solution that guarantees reusability at the block, core and system levels
- ☑ **Enhanced productivity:** Optimized for the latest verification process management and control capabilities of Cadence Incisive Enterprise

Further Information

For further information or to request an evaluation, please visit us online at www.globetechsolutions.com or call us at +30 23 10 31 35 53.

Component	Function
Serial Agent	Emulates the corresponding functionality of the serial device attached to the UART DUT by injecting data and control stimuli.
Monitor	Tracks activity on the network side of the UART device. It also provides error checking, data score-boarding and coverage information.

Note that the monitor element is required for all testing scenarios; all other elements are entirely independent and can be deployed separately.

Table 1: Functional Description of UART *e*VC Components

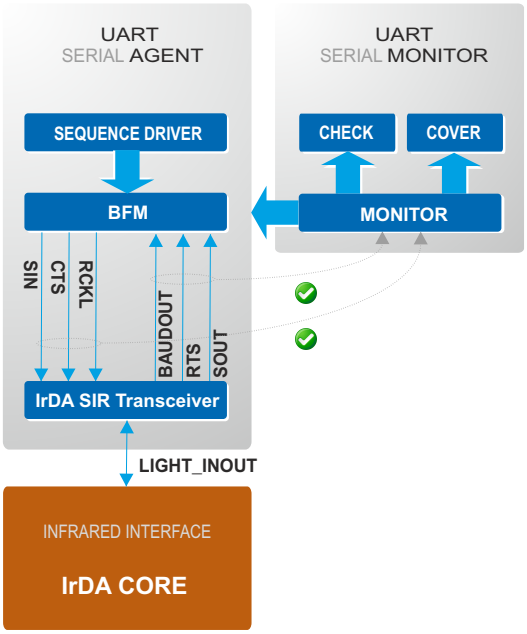

Figure 1: Verifying an SoC UART interface with the UART *e*VC
The Serial Agent is used to drive frames into the UART interface. The Monitor is used to check bidirectional communication and score board data on both the transmit and receive paths (not shown here).

Maturity	First Release	*e*RM Compliant	VPA Enabled	SB Optimized
Excellent	Sep 2003	✓	✓	✓

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