globetech SOLUTIONS

Verification Intellectual Property Products

IEEE 1149.1 (JTAG) *e*VC

e Verification Components

Globetech Solutions' *e*VCs are independent, pre-verified, re-usable, verification environments that can be readily integrated into your design.

Maintaining full compatibility with Cadence's Incisive Specman Simulator™, these components provide a solid basis for forming and realizing a complete, reliable and re-usable verification strategy.

e Reuse Methodology

Globetech Solutions' *e*VCs comply with Cadence's *e* Reuse Methodology (*e*RM™). The *e*RM ensures that *e*VCs seamlessly plug-and-play and operate consistently with all *e*RM compliant verification environments by applying consistent terminology, architecture, coding style and packaging.

Why *e*VCs?

There are many advantages to choosing a Globetech Solutions *e* Verification Component:

- **Time to silicon -** dramatically reduce the verification cycle
- **Flexibility -** quickly create and fine tune a variety of test scenarios
- **Risk Management -** pre-verified components help reduce problem space
- **Re-usability -** spend your time creating new tests, not environments!
- **Full Support -** integration, training and support to ensure your success

The IEEE 1149.1 (JTAG) *e*VC

In today's fast growing system-on-chip designs, incomplete or ineffective Design for Test support due to poor specification or loose design practices can quickly become the critical path to making market windows and delivering products within cost restrictions.

The IEEE JTAG *e*VC is a complete verification environment built around the IEEE 1149.1-2001 (JTAG) standard. Combine this *e*VC with the new IEEE 1500 *e*VC for a complete system-on-chip testability infrastructure verification solution.

Features

- ☑ Written in *e* and fully compatible with Cadence Incisive Specman Simulator - HDL independent
- ☑ *e*RM compliant - Plug-n-Play
- ☑ Includes executable verification plan for Incisive Verification Manager™
- ☑ Optimized for Incisive Scenario Builder™
- ☑ Fully compatible with the IEEE 1149.1-2001 Standard Test Access Port (TAP) and Boundary Scan Architecture (BSA) standard
- ☑ Sequence generation at different levels of abstraction including Transactions (e.g. load instruction) or Tests (e.g. EXTEST behavior)
- ☑ Integrated Bus Functional Model (BFM) complies to JTAG rules for transmission of test vectors and facilitates error injection
- ☑ Automated protocol and data checking at TAP ports and chain cells using an internal reference model (e.g. verify TCLK freeze)
- ☑ Support for verifying a daisy chain of an arbitrary number of JTAG TAPs and BSAs
- ☑ Functional coverage analysis view per single TAP or for complete TAP chain
- ☑ Pre-built support for arbitrary user-defined registers and instructions

The JTAG *e*VC Structure

The JTAG *e*VC comprises several components in compliance with *e* Reuse Methodology (*e*RM) for maximum interoperability and reuse (see **Table 1**).

Verification Using the JTAG *e*VC

From developing a JTAG TAP controller to designing a complete chip-level test architecture, the JTAG *e*VC can be a valuable tool for identifying design bugs, emphasizing protocol compatibility issues and ensuring smooth interoperability of testability features.

Figure 1 demonstrates how an *e*VC *Agent* can be used to verify a typical IC with JTAG support. All shift chains are automatically verified through the standard TAP. Furthermore, all boundary scan cells are exercised and checked for appropriate Capture, Update and Scan behavior.

The JTAG *e*VC is a scalable and extensible tool built on top of Cadence's industry leading Incisive Enterprise platform, bringing best-in-class verification methodologies to test's universal standard, with excellent reusability and return-on-investment.

Benefits of the JTAG *e*VC

- ☑ **Universal solution:** A powerful verification environment for the most widely accepted and used DFT standard
- ☑ **Proven quality:** In strict compliance with industry quality standards.
- ☑ **Maximum reuse:** An *e*RM-compliant solution that guarantees reusability at the block, core and system levels
- ☑ **Enhanced productivity:** Optimized for the latest Verification Process Automation products - Verification Manager and Scenario Builder
- ☑ **Advanced methodologies:** Part of Globetech's DFT Verification Kit™, a powerful set of tools and IP which can be used to automate verification of IEEE 1149.1 (BSDL) and 1450 (STIL/CTL) based DFT infrastructures

Further Information

For further information or to request an evaluation, please visit us online at www.globetechsolutions.com or call us at +30 23 10 31 35 53.

Component	Function
Agent	Provides the tools to exercise and examine IEEE 1149.1 DFT elements. The Agent can be Active or Passive and includes the Sequence Driver, BFM and Monitor modules.
Sequence Driver	Generates control and data at different levels of abstraction: Transactions (e.g. load instructions, go-to-reset) and Tests (e.g. EXTEST cell capture behavior, chain self-test).
Bus Functional Model (BFM)	Translates sequences into signal transactions with the JTAG TAP. Fully scalable and extensible.
Monitor	Monitors activity at the JTAG TAP as well as individual cell levels. The monitor deploys an IEEE 1149.1 reference model which is used for error condition detection. Each monitor is responsible for ensuring the smooth operation of a separate TAP in a chain test scenario.

Note that the monitor element is required for all testing scenarios; all other elements are entirely independent and can be deployed separately.

Table 1: Functional Description of IEEE 1149.1 (JTAG) *e*VC Components

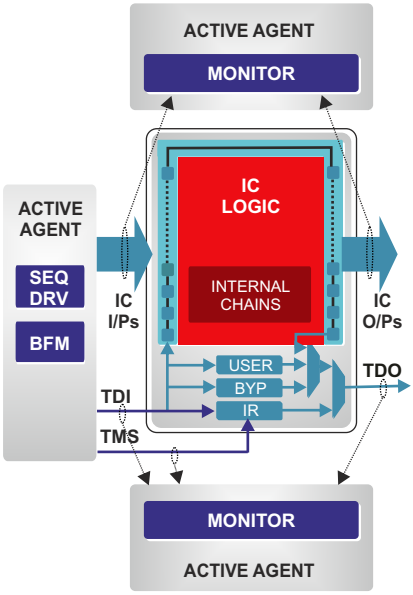

Figure 1: JTAG *e*VC Typical Operation
JTAG control and data signals are generated by the Agent, which also provides data for all cells' parallel inputs.

Maturity	First Release	*e*RM Compliant	VPA Enabled	SB Optimized
Excellent	Sep 2005	✔	✔	✔

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