globetech SOLUTIONS

Verification Intellectual Property Products

# IEEE1500 (SECT) *e*VC

## *e* Verification Components

Globetech Solutions' *e*VCs are independent, pre-verified, re-usable, verification environments that can be readily integrated into your design.

Maintaining full compatibility with Cadence's Incisive Specman Simulator™, these components provide a solid basis for forming and realizing a complete, reliable and re-usable verification strategy.

## *e* Reuse Methodology

Globetech Solutions' *e*VCs comply with Cadence's *e* Reuse Methodology (*e*RM™). The *e*RM ensures that *e*VCs seamlessly plug-and-play and operate consistently with all *e*RM compliant verification environments by applying consistent terminology, architecture, coding style and packaging.

## Why *e*VCs?

There are many advantages to choosing a Globetech Solutions *e* Verification Component:

- **Time to silicon -** dramatically reduce the verification cycle
- **Flexibility -** quickly create and fine tune a variety of test scenarios
- **Risk Management -** pre-verified components help reduce problem space
- **Re-usability -** spend your time creating new tests, not environments!
- **Full Support -** integration, training and support to ensure your success

## The IEEE1500 (SECT) *e*VC

The Standard for Embedded Core Test (SECT) *e*VC can verify a chain of one or more IEEE1500 compliant core wrappers. Whether developing a new test wrapper or integrating a third-party solution, the SECT *e*VC can be a valuable tool for identifying wrapper design bugs, bringing out protocol compatibility issues and ensuring smooth interoperability of testability features.

## Features

- ☑ Written in *e* and fully compatible with Cadence Incisive Specman Simulator - HDL independent
- ☑ *e*RM compliant - Plug-n-Play
- ☑ Includes executable verification and compliance plans for Incisive Verification Manager™
- ☑ Optimized for Incisive Scenario Builder™
- ☑ Fully compatible with the IEEE 1500-2005 Standard for Embedded Core Test, enabling complete DFT infrastructure verification
- ☑ Supports Serial/Parallel Test Access Mechanisms and multiple Cell Shift Stages
- ☑ Sequence generation at different levels of abstraction including primitives, instructions and tests (high-level compliance library)
- ☑ Integrated Bus Functional Model (BFM) complies to SECT rules for transmission of test vectors and optional injection of control signal errors
- ☑ Protocol and data checking at mandatory TAM ports using an internal reference model
- ☑ JTAG compatibility mode for SoC verification
- ☑ Support for verifying a daisy chain of multiple wrappers using multiple passive agents
- ☑ Automated support for arbitrary user-defined Registers (Wrapper Data Registers / Core Data Registers) and Instructions

## IEEE1500 (SECT) *e*VC Structure

The IEEE1500 (SECT) *e*VC employs an Agent as the key verification environment per IEEE1500 (SECT) wrapped core. The agent comprises three components: the Sequence Driver, the Bus Functional Model (BFM) and the Monitor. This structure allows for maximum flexibility in designing testing scenarios, as well as scalability, control and isolation (see **Table 1**).

## Verification Using the IEEE1500 (SECT) *e*VC

The IEEE1500 (SECT) *e*VC's powerful features and extensibility make it unique for verifying designs that employ one or an arbitrary number of IEEE1500 wrapped cores in isolation or chained together, providing full metrics for error conditions and functional coverage.

As illustrated in **Figure 1**, a typical IEEE 1500 wrapper consists of a set of mandatory (WIR, WBY, WBR) and user defined registers (e.g. WDR, CDR). Furthermore, the wrapper can be operated using either the mandatory (serial WSI/WSO) or an optional (e.g. parallel WPI/WPO) Test Access Mechanism (TAM).

The IEEE1500 *e*VC's extensible *e*RM-compliant architecture supports a large range of wrappers, instructions and user-defined registers, harnessing the scalability of the IEEE1500 standard. The *e*VC already provides all the necessary building blocks to help accelerate and automate verification; predefined primitives, instruction and test sequences, automated checks and conclusive functional coverage information.

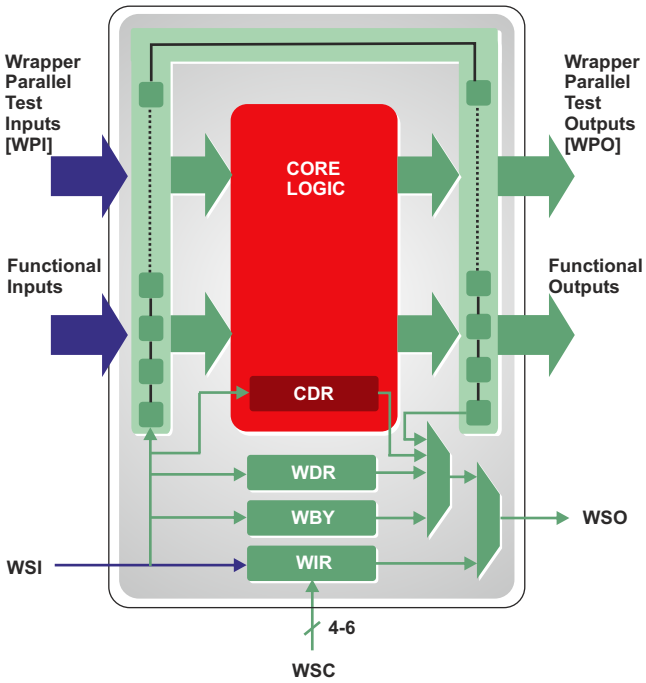



Figure 1: Typical Standalone IEEE1500 (SECT) Wrapped Core

| Component | Function |
|---|---|
| **Agent** | Models a Standard IEEE1500 Serial Access and Control Source and Sink. The Agent can be Active or Passive and includes the Sequence Driver, BFM and Monitor modules. |
| **Sequence Driver** | Generates control and data at different levels of abstraction: Primitives (e.g. SHIFT_WIR), Instructions (e.g. WS_ExTest) and Tests (high-level IEEE1500 compliance library). |
| **Bus Functional Model (BFM)** | Capable of driving wrapper control and data input signals with data passed by the Sequence Driver. Can operate in either IEEE1500 (CTAG) native or IEEE1149.1 (JTAG) mode. Fully scalable and extensible. |
| **Monitor** | Capable of monitoring activity on all wrapper control and data signals for error checking and coverage collection. The monitor implements an IEEE1500 reference model which is used for error condition detection. Each monitor is responsible for ensuring the smooth operation of a separate wrapper in a chain test scenario. |
| Note that the monitor element is required for all testing scenarios; all other elements are entirely independent and can be deployed separately. | |

Table 1: Functional Description of IEEE1500 (SECT) *e*VC Components

## IEEE1500 *e*VC Supported Operations

In its base configuration, the IEEE1500 *e*VC supports all mandatory and conditionally mandatory protocol signals and instructions (see **Table 2**), hence complying as a standard *Serial Access and Control Source/Sink*. In addition, it supports several optional instructions and modes, such as parallel test data insertion.

When in serial mandatory mode, the *e*VC can control and inject vectors into virtually any IEEE1500 Wrapped Core, whether it is developed in-house or procured from an external supplier. Furthermore it can perform a series of consistency and functionality tests on the wrapper, as well as generate useful coverage metrics for quality assessment and project progress management.

Taking advantage of the simple but powerful SECT constructs, the SECT *e*VC can provide a fast and reliable way of ensuring the proper functional behavior and protocol adherence of developed, generated or procured IEEE 1500 wrapped IP.

| Instruction | Mode |
|---|---|
| **WS_Bypass** | Wrapper in bypass (functional mode). WSI and WSO are connected through WBY. |
| **W[*S,P*]_ExTest** | Test of external circuitry through a serial or parallel TAM |
| **W[*S,P*]_InTest_ [*Scan, Ring*]** | Internal core testing through a serial or parallel TAM |
| **W[*S,P*]_Preload** | If defined, loads data into the dedicated shift path of WBR. |
| **WS_Safe** | If defined, drives a safe value out of WBR cells |

Table 2: IEEE1500 *e*VC Base Supported Instructions

## The SECT *e*VC Agent

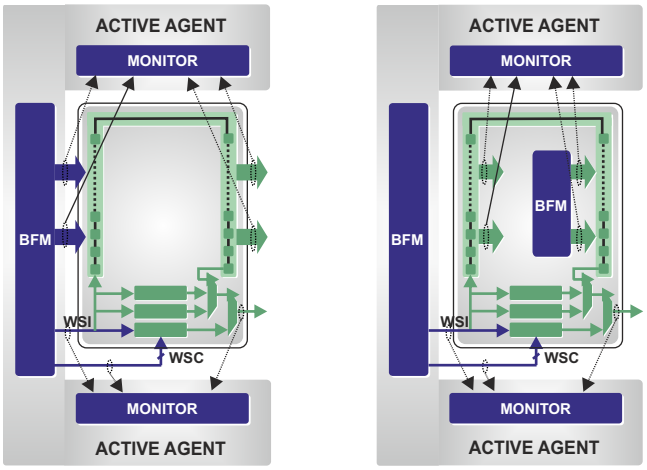
The main functional component of the SECT *e*VC is the *Agent*. An Agent can be *Active* or *Passive* depending on whether or not it can drive data into the wrapper under test. Depending on the user configuration, the Active Agent can drive data into the test inputs of the wrapper (WSI/WPI) and, optionally, into the functional inputs of the wrapper, depending on the instruction and test mode (see **Figure 2**).

In **Figure 2(a)**, the Wrapper Boundary Register (WBR) is programmed facing *outwards* by means of selecting one of the external test instructions. The *e*VC will automatically drive all external inputs and observe all external outputs respectively, making valuable consistency checks.

In **Figure 2(b)**, the WBR is programmed facing *inwards* by means of selecting one of the internal test instructions. The *e*VC now drives and observes internal inputs only.

Note that the flexible architecture of the SECT *e*VC allows this type of inward/outward behavior in order to be easily driven and monitored for all mandatory and user-defined registers.

Furthermore, vector generation is made simple and powerful by including a set of predefined sequences, capable of generating transactions at different levels of abstraction with minimal effort.




(a) Outward (External Test) (b) Inward (Internal Test)

**Figure 2: SECT *e*VC Operation for Different WBR orientations**
The BFM optionally drives cells which subscribe to *Capture* behavior.

## JTAG Mode

One of the most useful features of the IEEE1500 testability standard is its well-designed compatibility with the existing, dominant, IEEE1149.1 (JTAG) standard. In order to provide the user with all the necessary tools to effectively verify a chip with an external JTAG interface, the IEEE1500 *e*VC allows the Agent to run in *JTAG Compatibility Mode*. When in this mode, the Agent will generate the appropriate JTAG control signal, TMS, instead of the IEEE1500 control signals, WSC (see **Figure 3**). Toggling between IEEE1500 and IEEE1149.1 modes is part of the *e*VC configuration and does not require any test changes or additional *e* code.

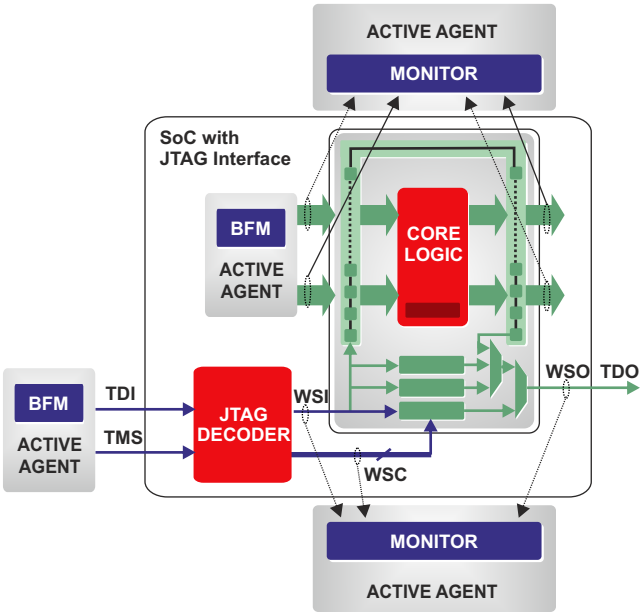



**Figure 3: SECT *e*VC Operation in JTAG Mode**
The BFM optionally drives JTAG control and data signals.

The *e*VC monitor continues checking the wrapper for data errors and collecting coverage information.

For additional JTAG verification capabilities, please refer to the IEEE 1149.1 (JTAG) *e*VC by Globetech Solutions.

## User-defined Extensions

The IEEE1500 *e*VC provides complete support for user-defined extensions in the form of registers and instructions.

A user-defined register can be an internal core register or a wrapper register and can be associated with several user-defined instructions. Typical examples include embedded testability features such as internal memory BIST controllers, ATPGs, etc.

The SECT *e*VC cleverly subtypes its basic register definitions in order to support automatic data checks, generation and functional coverage capabilities for the new extensions. Furthermore, the user can extend these base capabilities, adding support for virtually any type of IEEE1500-compliant entity, along with enhanced data checking and functional coverage collection.

## Support for Mixed Registers

Mixed registers are registers which can include both dedicated scan cells as well as cells from other registers. An example of such a register is the WS_InTest_Scan instruction for internal testing, which connects WSI to WSO through the WBR and internal core scan chains.

The SECT *e*VC supports such fully or partially *Virtual* registers by cross-linking scan structures together and hence providing arbitrary flexibility in implementing new instructions.

## Verifying a Chain of IEEE 1500 Wrapped Cores

When used to verify a chain of IEEE1500 wrapped cores, the SECT *e*VC maintains all the features that are available to the verification engineer in the case of single wrapper verification.

This is achieved by creating **multiple instances** of the *e*VC Agent and configuring them as a single Active Agent array (see **Figure 4**). The Active Agent is able to drive and observe the head of the wrapper chain (note that this can also be done in JTAG mode in the presence of a JTAG decoder). A *Passive* Agent is then instantiated and assigned to each remaining wrapper in the chain, capable of observing its respective wrapper.

## Further Information

For further information or to request an evaluation, please visit us online at www.globetechsolutions.com or call us at +30 23 10 31 35 53.

## Benefits of the IEEE 1500 *e*VC

- ☑ **Emerging Technology:** A complete verification solution for the future standard of DFT technology.
- ☑ **Advanced Capabilities:** Enables coverage-driven verification flows for any IEEE 1500 compliant wrapper infrastructure.
- ☑ **Maximum reuse:** An *e*RM-compliant solution that guarantees reusability at the block, core and system levels
- ☑ **Enhanced productivity:** Optimized for the latest Verification Process Automation products - Verification Manager and Scenario Builder
- ☑ **Advanced methodologies:** Part of Globetech's DFT Verification Kit™, a powerful set of tools and IP which can be used to automate verification of IEEE 1149.1 (BSDL) and 1450 (STIL/CTL) DFT infrastructures.

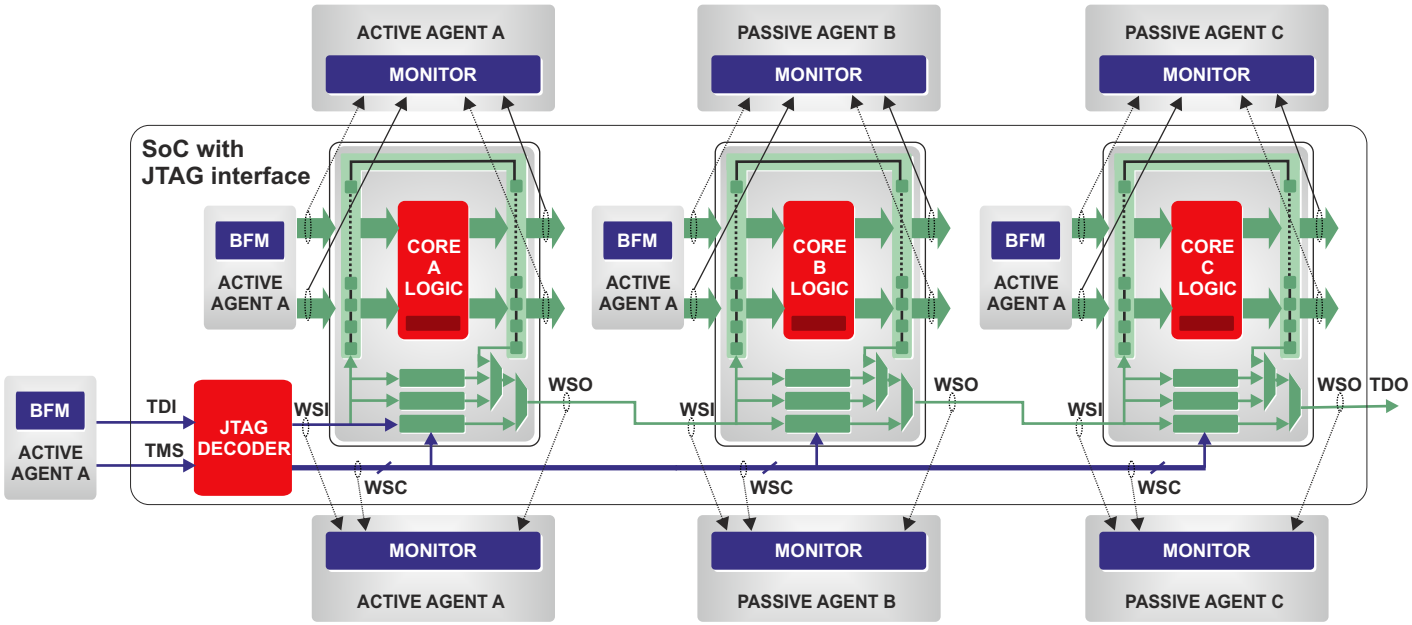



**Figure 4: Verifying a chain of IEEE1500 wrapped cores using the SECT *e*VC in JTAG Mode and multiple Agent instances.**

| Maturity | First Release | *e*RM Compliant | VPA Enabled | SB Optimized |
|---|---|---|---|---|
| Good | Jun 2005 | ✓ | ✓ | ✓ |


globetech SOLUTIONS

66 G.Viziynou St
Thessaloniki
54636 Greece
Tel: +30 23 10 31 35 53
Fax: +30 23 10 31 39 64
info@globetechsolutions.com
www.globetechsolutions.com